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10EC56

Fifth Semester B.E. Degree Examination, Dec. 2013 / Jan 2014.
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART - A

1 a. Explain the fabrication steps of CMOS P – well process with neat diagram and write the mask sequence. **(12 Marks)**

b. List the threshold voltage equations and emphasize each term. **(08 Marks)**

2 a. Write the CMOS inverter circuit and briefly explain. Write the CMOS VTC showing regions A, B, C, D, E. Derive the expressions for output voltage in region 'B'. **(10 Marks)**

b. Write the circuit and layout for $Y = \overline{AB + CD + E}$ in CMOS style. **(10 Marks)**

3 a. Write the circuit and stick diagram for CMOS tristate inverter. **(04 Marks)**

b. Write the circuit of Bi CMOS NAND and NOR gate and briefly explain. **(08 Marks)**

c. Explain the circuit of dynamic CMOS logic by taking an example of the function $Y = \overline{A(B+C)+DE}$. **(08 Marks)**

4 a. Define Sheet Resistance (Rs) and standard unit of capacitance (□Cg). Calculate the on resistance of 4:1 nmos inverter with Rs = 10kΩ/□, $Z_{pu} = \frac{8\lambda}{2\lambda}$, $Z_{pd} = \frac{2\lambda}{2\lambda}$. Also estimate the total power dissipated if V_{DD} = 5V. **(08 Marks)**

b. Calculate the capacitance in □ Cg for the given metal layer shown in fig.Q4(b), if feature size = 5μm and relative value of metal to substrate = 0.075. **(05 Marks)**

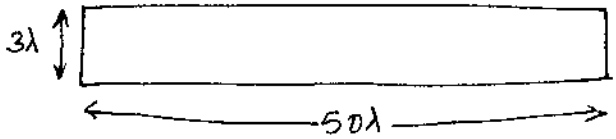

Fig.Q4(b)

c. Explain briefly the circuit of inverting and non – inverting super buffer. **(07 Marks)**

PART - B

5 a. Calculate the O/P voltage V_{out} in the circuit given below for different values of V_a, V_b. **(04 Marks)**

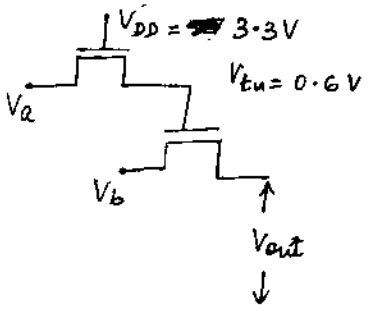

Fig.Q5(a)

V_a	V_b
3·3	3·3
1·5	1·5
3·3	0
0	1·5

b. Design Bus Arbitration logic for n – line bus. **(10 Marks)**

c. Consider λ – based design rules and 5μm technology. How many nmos 8:1 inverter $\left(Z_{pu} = \frac{16\lambda}{2\lambda} \text{ and } Z_{pd} = \frac{2\lambda}{2\lambda}\right)$ can be driven by a minimum size conductor which is 3λ wide and 1μm thick? Assume $J_{th} = 1mA/(\mu m)^2$, $R_s = 10K\Omega / \square$, $V_{DD} = 5V$. **(06 Marks)**

6 a. Discuss the 4 phase clocking scheme to avoid the problem of cascading in dynamic CMOS logic. **(06 Marks)**

b. What are the adder enhancement techniques? Briefly explain. **(04 Marks)**

c. Write and explain 6 – bit carry select adder. **(10 Marks)**

7 a. Write and explain 4 Transistor dynamic and 6 Transistor static CMOS memory cell with sense amplifier. **(12 Marks)**

b. Explain the one transistor dynamic memory cell emphasizing three plate capacitor. **(08 Marks)**

8 Write short notes on :

a. Latch up. **(07 Marks)**

b. Nature of failures in CMOS. **(06 Marks)**

c. I/O pads. **(07 Marks)**

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